WE CLAIM:

1. A liquid crystal display with a large pixel aperture ratio comprising:

a liquid crystal layer sandwiched between first and second substrates;

an array of thin film transistors and corresponding pixel electrodes mounted on said first substrate, each of said thin film transistors including a semiconductor layer, a gate electrode connected to a gate address line, a drain electrode connected to a drain address line, and a source electrode connected to one of said corresponding pixel electrodes, and wherein said pixel electrode connected to said source electrode overlaps said gate and drain address lines along longitudinal edges thereof; and

a substantially continuous insulating layer having a dielectric constant ϵ no greater than about 3.0 disposed between said pixel electrode and said address lines in sufficient thickness so as to reduce capacitive cross-talk in the display by reducing the pixel electrode-address line parasitic capacitance C_{PL} in the areas of overlap.

2. The liquid crystal display of claim 1, wherein C_{PL} is defined by the equation:

$$C_{PL} = \frac{\epsilon \cdot \epsilon_0 \cdot A}{d}$$

where ϵ_0 is 8.85×10^{-14} F/cm, "d" is the insulating layer thickness in the overlap areas, and "A" is the area of the capacitor formed between said pixel electrode and said address lines in the overlap area; and

wherein C_{PL} is less than or equal to about 0.01 pF when the pixel pitch of the display is about 150 μm so as to reduce cross-talk in the display.

3. The liquid crystal display of claim 1, wherein the insulating layer thickness "d" is at least about 1.5 μm in the overlap areas.

4. The liquid crystal display of claim 3, wherein "d" is from about 2 to 3 μm in the overlap areas and said insulating layer has a degree of planarization of at least about 90%.

5. The liquid crystal display of claim 3, wherein the display has a pixel aperture ratio of at least about 65%, and a pixel pitch of from about 40 to 500 μm.

6. The liquid crystal display of claim 5, wherein said pixel aperture ratio is at least about 75%.

7. The liquid crystal display of claim 1, wherein said pixel electrode overlaps said gate and drain address lines along substantially their entire lengths so as to increase the pixel aperture ratio of the display.

8. The liquid crystal display of claim 1, wherein at least one via is defined for each pixel in said insulating layer so that said pixel electrode can be electrically connected to said source electrode through said via.

9. The liquid crystal display of claim 8, wherein said insulating layer defines another via for each pixel so that said pixel electrode can also be connected to a storage capacitor electrode through said another via.

10. The liquid crystal display of claim 1, wherein said insulating layer includes Benzocyclobutene (BCB) and has a dielectric constant ϵ of about 2.7 or less.

11. The liquid crystal display of claim 1, wherein said pixel electrode overlaps said address lines along their lengths by at least about 0.5 μm.

12. The liquid crystal display of claim 1, wherein said semiconductor layer is intrinsic amorphous silicon and is disposed between (i) said gate electrode and (ii) said source and drain electrodes.

13. The liquid crystal display of claim 12, wherein said pixel electrode is ITO and said drain electrode is Mo.

14. A thin film transistor (TFT) structure comprising:

a substantially transparent substrate;

a gate electrode located on said substrate and adapted to be connected to a first address line;

a semiconductor layer located on said substrate over said gate electrode;

a drain electrode located on said substrate over said semiconductor layer and adapted to be connected to a second address line;

a source electrode located on said substrate over said semiconductor layer and spaced from said drain electrode so as to define a transistor channel, said source electrode adapted to be electrically connected to a pixel electrode;

an insulating layer located on said substrate over said source and drain electrodes, said insulating layer being of sufficient thickness "d" and having a

sufficiently low dielectric constant value ϵ so that when said pixel electrode overlaps one of said first and second address lines, the resulting pixel electrode-address line parasitic capacitance C_{PL} is sufficiently low so as to substantially eliminate cross-talk.

15. The TFT structure of claim 14, wherein said insulating layer is at least about 1.5 μm thick in areas where the pixel electrode overlaps one of said address lines.

16. The TFT structure of claim 14, wherein said insulating layer includes Benzocyclobutene (BCB) and has a dielectric constant ϵ of less than about 3.0.

17. The TFT structure of claim 14, wherein said insulating layer has a dielectric constant of less than about 3.0, a thickness of at least about 1.5 μm in the overlap areas, and C_{PL} is no greater than about 0.01 pF.

18. A method of making a liquid crystal display including an array of TFTs, the method comprising the steps of:

providing a substantially transparent first substrate;

disposing a gate metal layer on said first substrate and patterning an array of TFT gate electrodes and gate address lines therefrom;

disposing a semiconductor layer on said first substrate over said gate electrodes and patterning the semiconductor layer to form TFT areas;

disposing and patterning drain and source electrodes on said substrate over the semiconductor layer;

providing drain address lines for addressing the drain electrodes;

disposing a substantially continuous organic insulating layer on said substrate over said address lines and said drain and source electrodes to a thickness of at least about 1.5 μm; and

disposing and patterning an array of substantially transparent pixel electrodes on said substrate over said insulating layer so that the patterned pixel electrodes overlap at least one of said gate and drain lines in order to increase the display's pixel aperture ratio.

19. The method of claim 18, further comprising the step of making the display so that the resulting pixel electrode-address line parasitic capacitance C_{PL} defined in the overlap areas is no greater than about 0.01 pF when the pixel pitch of the display is about 150 μm.

20. The method of claim 18, wherein the insulating layer is made substantially of Benzocyclobutene (BCB) and has a dielectric constant ϵ less than about 3.0.

21. A liquid crystal display comprising:

a liquid crystal layer;

a substantially transparent substrate adjacent said liquid crystal layer;

an array of thin film transistors disposed on said substrate, said thin film transistors connected to address lines and acting as switching elements for energizing corresponding pixel electrodes;

a substantially transparent planarization layer disposed on said array of transistors, said planarization layer being located between (i) said pixel electrodes; and (ii) said address lines; and

wherein said planarization layer includes Benzocyclobutene (BCB) and has a dielectric constant of less than about 3.0.

22. The display of claim 21, wherein said pixel electrodes overlap at least some of said address lines in order to increase the pixel aperture ratio of the display, and said planarization layer is at least about 1.5 μm thick in the areas of overlap so as to minimize the parasitic capacitance created in the overlap areas between the pixel electrodes and the address lines.